AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 14, line 10 through page 15, line 7 as shown.

Further, processor 401 includes a watchpoint controller 403 that provides control information to a pipeline control unit 409 in order to stall and start an execution pipeline of processor 401. The watchpoint controller 403 may also keep track of watchpoint channel information in processor 401, and provide such information to circuit 402. Processor 401 also includes a branch unit 404 that handles branch-related instructions in processor 401, resolves/predicts branch addresses, and other branch-related functions. Branch unit 404 provides signals program counter information 414, CPU mode information 415, and branch information 416. Branch unit 404 also provides process identifier or ASID information[[416]] 421. Processor 401 also includes a load-store unit 405 which is responsible for performing execution functions. Load-store unit 405 includes operand address (OA) watchpoints 406, which produce operand address information[[415]] 423.

ASID information[[416]] 421 and operand address (OA) information[[415]] 423 are fed through multiplexer[[417]] 422 and transmitted to debug circuit 402 via data line 417. In one aspect of the invention, it is understood that when new ASID information[[416]] 421 is available, no operand address information[[415]] 423 will be available concurrently. Thus, the number of communication lines in communication link 420 are reduced because both ASID information[[416]] 421 and OA information[[415]] 423 are transmitted alternately over the same communication lines.

Please amend the fourth paragraph on page 18, lines 21 through 28 as shown.

Further, branch unit 507 may provide ASID information Sr.asid 515 every time that there is an ASID update. In one embodiment of the invention, sr.asid signal 515 is multiplexed with operand address watchpoint information[[522]] 523 to produce p_dm_data 516. In one embodiment, there can be no clash between the transmission of ASID information and other trace data, because ASID updates occur after a return from exception (RTE) instruction reaches the writeback stage of execution. Because the RTE instruction is a back-serialized instruction, there will be no instructions in the pipeline until after the RTE instruction has completed.